MEMORY ARCHITECTURE WITH MEMORY CELL GROUPS

Abstract of Disclosure

An improved cell design for series memory architecture is disclosed. The improved cell design facilitates the formation of capacitors using a single etch process instead of two, as conventionally required. In one embodiment, each capacitor of a capacitor pair is provided with at least one plug contacting a common diffusion region of two adjacent cell transistors. In another embodiment, a large plug with sufficient overlap to the bottom electrodes of pair of capacitors is used.

Figures